SECTION II

MAINTENANCE CHECKS AND ADJUSTMENTS

2. INTRODUCTION

This section is for the use of the OEM Repair Department. It contains checks and adjustments that are used during the normal life of the drive.

Before applying power to the drive or doing any checks or adjustments, visually inspect the drive to ensure that it has no missing or broken parts.

The following equipment is required for checks and adjustments:

1. A dual-channel, wideband oscilloscope: Tektronix 465 or equivalent
2. An exerciser or software routine capable of stepping the drive to any track, selecting the upper or lower head, and writing a 1F, all zeros if FM,or a 2F, all ones if FM, pattern on the disk.
3. A Phillips screwdriver
4. A set of Allen wrenches
5. A flat blade screwdriver
6. A blank diskette
7. An alignment diskette: Dysan P/N 360/2A or equivalent
8. Integrated circuit dip clips, 14 and 16 pin

2.1 SPINDLE DRIVE MOTOR CHECKS AND ADJUSTMENTS

The long-term drive motor speed adjustment ensures that the motor's speed is within the range of tolerance specified. The motor speed specification is 360 RPM ± 1.25 percent.

2.1.1. Long-Term Drive Motor Speed Checks and Adjustments

A. Preliminary checks required:

Verify power: +24V D. C. ±10 percent
+5V D. C. ± 5 percent

B. Apply power to the drive.

C. Activate the drive motor on the interface line.

D. Insert a work diskette.

E. Set up the oscilloscope, as follows:

Voltage: 2 volts per division

Time Per Division: 20 milliseconds

Trigger: Negative, Channel A, R33

Note

For the TM848-1 single-sided drive, trigger off of R33. For the TM848-2 double-sided drive, trigger off of Test Point 12, with the exception of azimuth, which must be triggered off of R33 (see Figure 2-1).

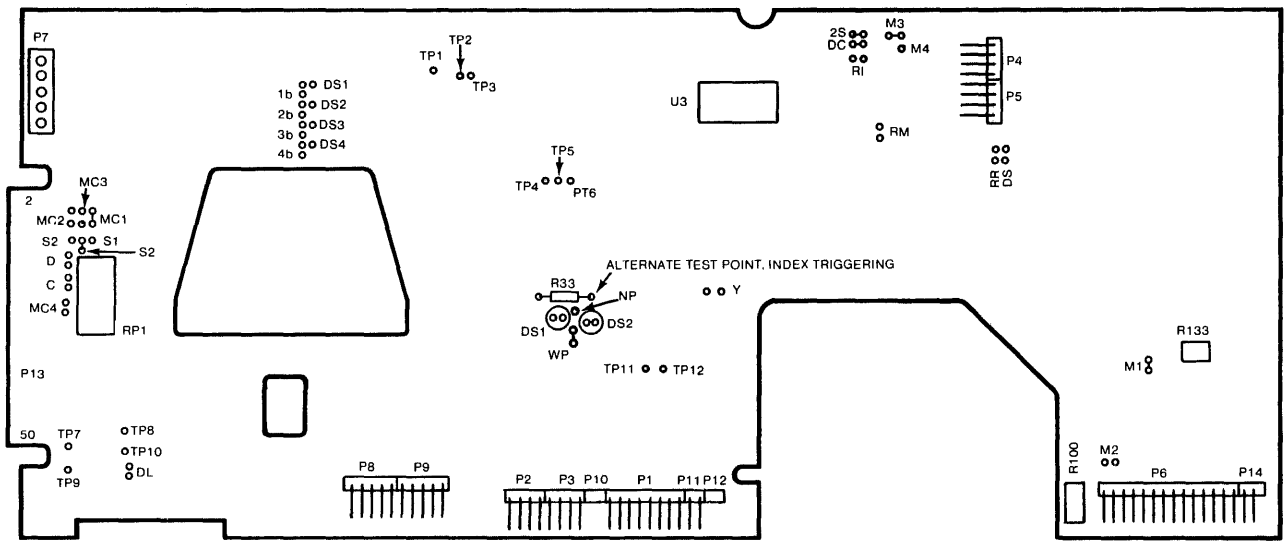


Figure 2-1
Circuit Board Assembly

F. Adjust R133 until a reading of 166.667 milliseconds is achieved from leading edge to leading edge of the index pulses.

G. If the drive motor's speed cannot be adjusted, see Section IV, Troubleshooting Guide.

2.2 CATS EYE ALIGNMENT CHECK AND ADJUSTMENT

The Cats Eye (C. E.) alignment procedure locates the read/write head at the proper radial distance from the hub center line, ensuring that the track location is accurate (see Figure 2-2). This adjustment is necessary only after servicing or if diskette interchange problems are suspected.

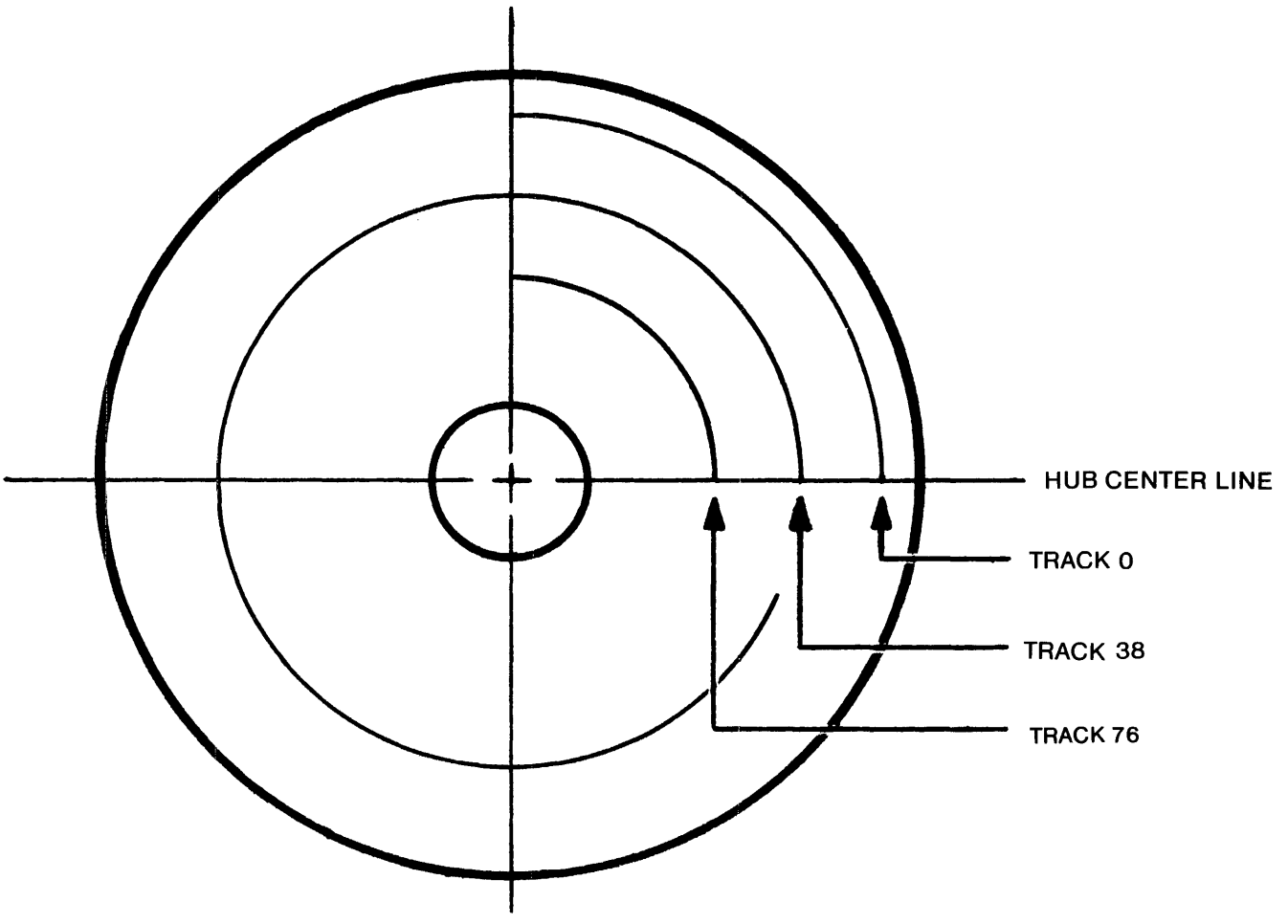


Figure 2-2
Hub Center Line and Track Locations

2.2.1 Cats Eye Alignment Check

A. Set up an oscilloscope, as follows:

Channel A;	Test Point 2 alternate is Test Point 4 on R30
Channel B:	Test Point 3 alternate is Test Point 5 on R29
Ground	Test Point 1
Read Differentially:	A plus B, B inverted
Time Base:	20 milliseconds per division
External Trigger:	Test Point 11, negative trigger, for single-sided drives. Test Point 12, negative trigger, for double-sided drives. R33 (end closest to DS2), negative trigger, is an alternate test point for both single- and double-sided drives.

B. Apply power to the drive.

Note

The Track 38 radius is 2.8207 ± .0020. Other track locations are computed based upon 48TPI.

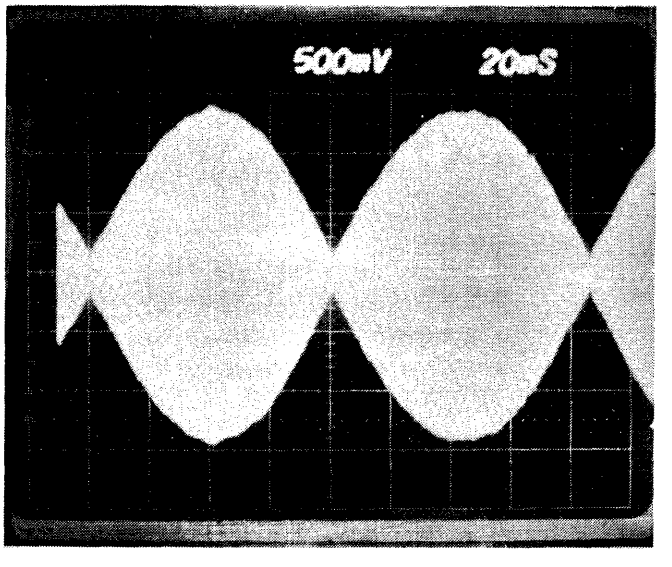
C. Select the drive at the interface.

D. Insert the alignment diskette into the drive.

E. Select Head 00, the lower head.

F. Seek to and observe Track 38 for Cats Eye alignment of the lower head.

G. Adjust the oscilloscope to observe a Cats Eye pattern (see Figure 2-3).



Equal amplitude.
Lobes shown at 100 percent on Track 38.

Time Scale: 20 ms

Figure 2-3
Cats Eye Pattern

H. Verify that the smaller of the two Cats Eye lobes is not less than 75 percent in amplitude of the other one. The calculation is: $\frac{\text{amp of smaller lobe}}{\text{amp of larger lobe}} \times 100$

I. Step the drive to Track 00, then, step it back to Track 38.

J. Reverify the Cats Eye pattern.

K. Step the drive to Track 76; then, step it back to Track 38.

L. Reverify the Cats Eye pattern.

M. On double-headed drives, select the upper head (Head 01) and repeat Steps F through L.

N. If any of the checks listed above does not meet the conditions stated in Step H, the head carriage must be adjusted.

2.3 HEAD CARRIAGE ADJUSTMENT

A. Turn the two position retaining screws that straddle the nylon adjustment cam located beneath the drive until the cam can be moved (see Figure 2-4).

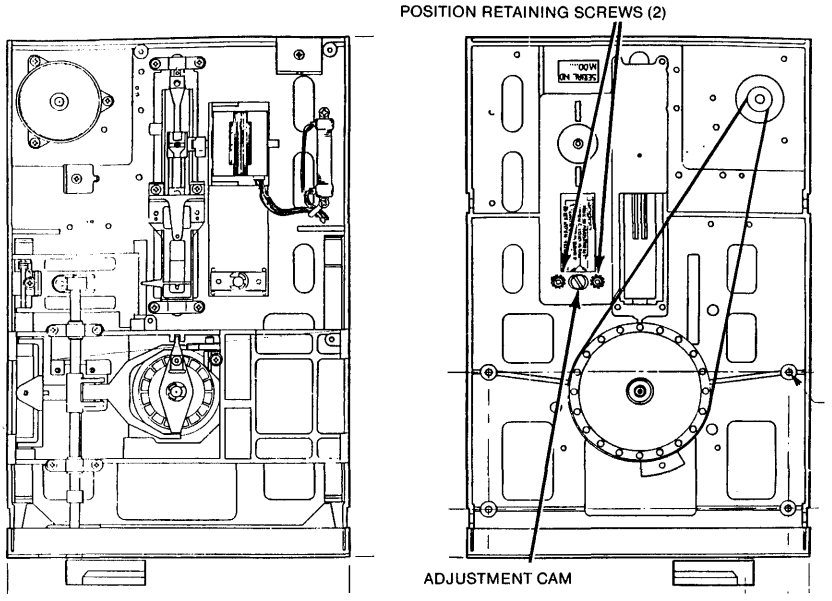


Figure 2-4

Head Module Retaining and Cam Screws

B. Observe the Cats Eye pattern from the head that is farthest out of alignment.

C. Using a flat blade screwdriver, turn the adjustment cam until one Cats Eye lobe is within 75 percent of the amplitude of the other lobe.

Note

Check the upper and lower heads on double-sided drives (see Section 2.2.1, "F" through "L" on upper head).

D. Tighten the two positioner retaining screws (see Figure 2-4).

E. Reverify the Cats Eye alignment (see Section 2.2.1).

2.4 INDEX SENSOR CHECKS AND ADJUSTMENTS

The index adjustment changes the time period from the index pulse to the start of the data. The adjustment should be checked after the drive has been aligned (see Section 2.1.1) or when diskette interchange errors are suspected.

2.4.1 Index-to-Data Burst Check

A. Apply power to the drive.

B. Select the drive.

C. Check the spindle speed of the drive (see Section 2.1).

D. Set up an oscilloscope as follows:

Trigger:	Single-sided drives trigger on right lead of R33 (closest to DS2), negative edge; double-sided drives trigger on Test Point 12, negative edge.
Read Differentially:	A plus B, B inverted
Channel A:	Test Point 2
Channel B:	Test Point 3
Time Base:	50 microseconds per division

E. Insert an alignment diskette.

F. Seek to Track 1.

G. Select Head 00, the lower head.

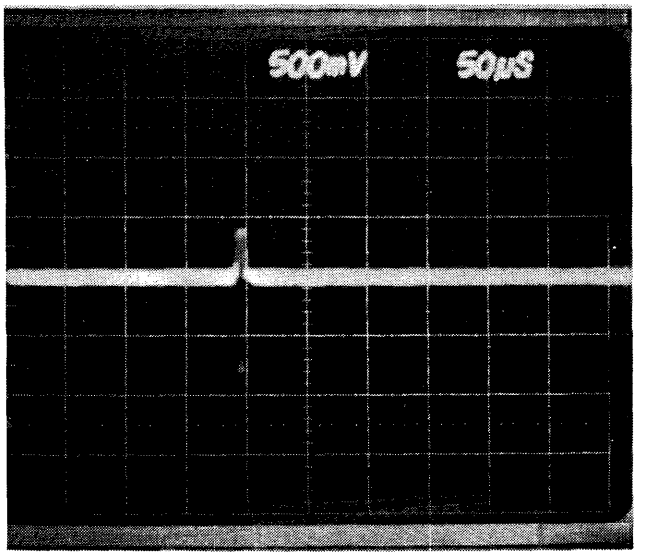
H. Ensure that the index-to-data burst occurs at 200 microseconds ± 100 microseconds from the leading edge of the index pulse (see Figure 2-5).

I. For double-sided drives, select Head 01 and repeat the steps above.

Note

Head 01 should meet the same specification.

J. If either Head 00 or Head 01 does not meet the specifications, adjust the index sensor (see Section 2.4.2.).



Time Scale:
50 usec per
division

Figure 2-5
Index-to-Data Burst

K. When both index measurements on a double-sided drive or the one index measurement on a single-sided drive meet the specifications, see Section H, check the index-to-data burst on Track 76.

L. On a double-sided drive, check Heads 01 and 00, the upper and lower heads.

Note

If any index measurement does not meet the specification, the index sensor must be adjusted (see Section 2.4.2).

2.4.2 Index Sensor Adjustment

A. Loosen the index sensor's retaining screw located on the underside of the chassis (see Figure 2-6).

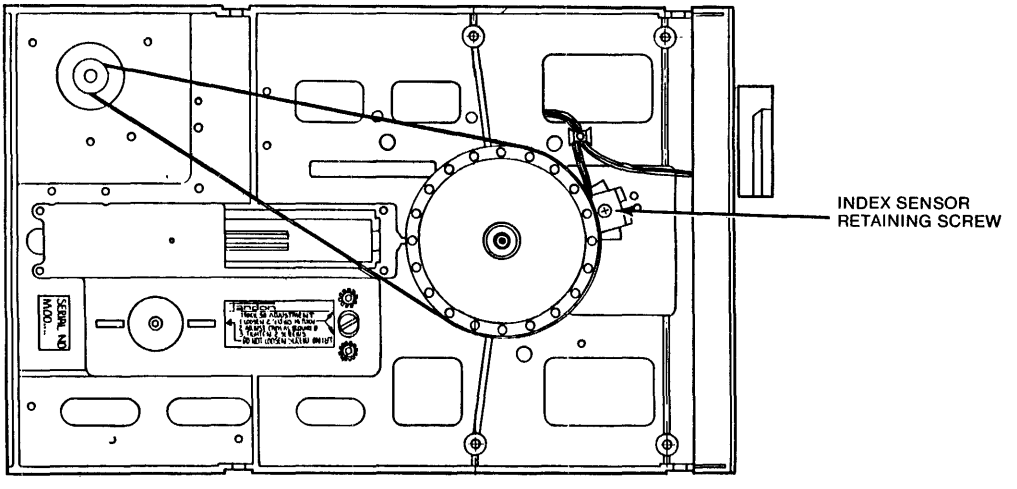


Figure 2-6
Index Sensor's Retaining Screw and Adjustment

B. Adjust the index sensor with a flat blade screwdriver until the index-to-data burst occurs 200 microseconds ± 100 microseconds from the leading edge of the index pulse.

C. Tighten the index sensor's retaining screw.

D. Reverify the index-to-data bursts (see Section 2.3.1).

2.4.3 Index Pulse Width Check

The index pulse width is nonadjustable. If the index pulse width is not within specifications, replace the Index Sensor Assembly.

A. Set up an oscilloscope as follows:

Channel A:	To appropriate index test point, see Section 2, Item Number 1.
Ground:	Test Point 1
Time Base:	.5 millisecond per division
Voltage:	2 volts per division
Trigger:	Negative leading edge of Channel A, appropriate test point.

B. Ensure that the negative going pulse width is between 1.0 and 2.3 milliseconds (see Figure 2-7).

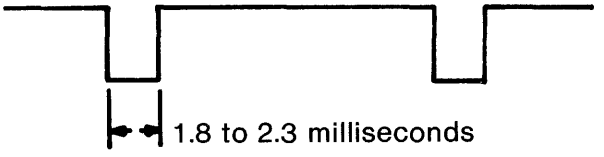


Figure 2-7
Negative Going Pulse Width

2.5 TRACK 00 SENSOR CHECK AND ADJUSTMENT

The Track 00 sensor provides a signal that identifies Track 00 to the logic electronics. A Track 00 signal is sent to the controller on Pin 20 of the interface.

A. Apply power to the drive.

B. Load an alignment diskette into the drive.

C. Step the carriage to the radial alignment track, Track 38 (see Section 2.2).

D. Confirm the position by observing the Cats Eye pattern.

E. Attach Channel A to Test Point 10.

F. Restore the carriage to Track 00, and ensure that the Track 00 L. E. D. on the exerciser turns on.

G. Seek to Track 1, and ensure that the signal at Test Point 10 is high.

H. Seek to Track 2, and ensure that this line is low or in transition.

I. Seek to Track 3, and ensure that this line is low.

J. If the signal is incorrect, restore to Track 00 with the oscilloscope attached as above.

K. Seek out to Track 2, and loosen the two retaining screws that hold the Track 00 sensor (see Figure 2-8).

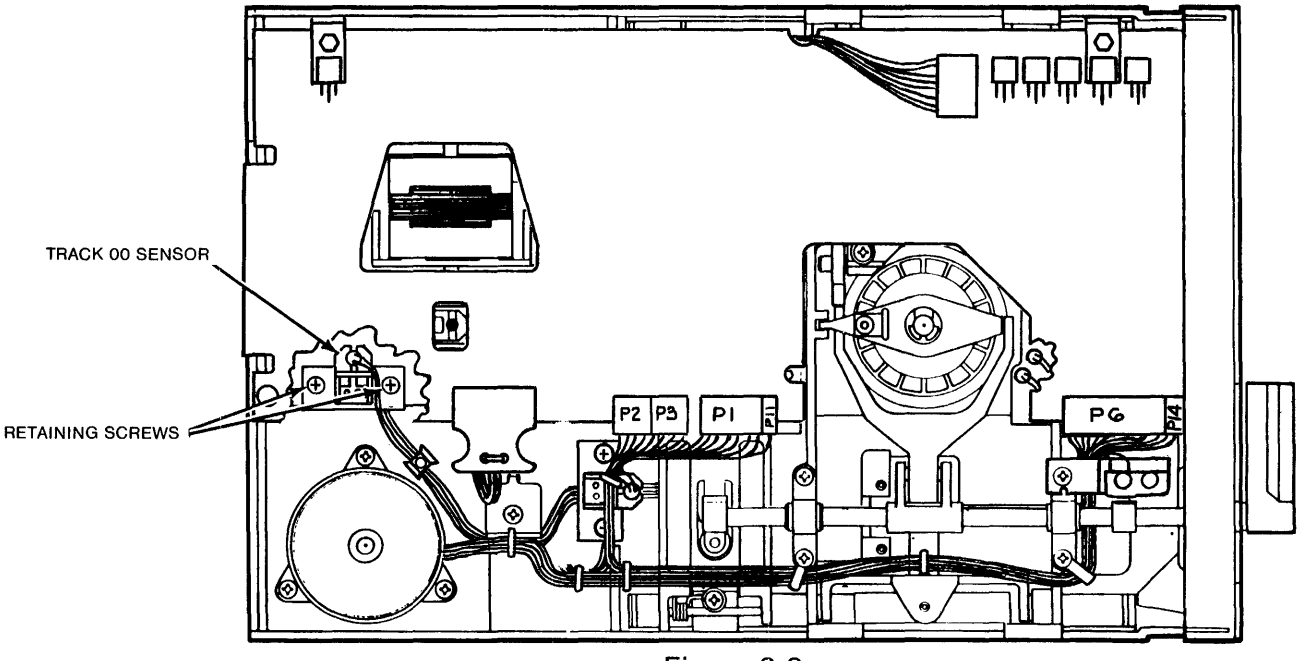


Figure 2-8
Track 00 Sensor

L. Push the sensor toward the back of the drive, and slowly push it forward until the signal on the oscilloscope just goes low (true).

M. Tighten the retaining screws, and repeat Steps E through I.

N. Verify the adjustment.

2.6 AMPLITUDE CHECK

The amplitude test checks the necessary read, channel amplifier/differential output voltage.

A. Restore to Track 00

B. Insert a work diskette and write a 2F, all ones, pattern on the lower head.

C. Connect an oscilloscope to Test Points 4 and 5, using Test Point 1 as a ground.

D. Set up an oscilloscope as follows:

Channel A:	Test Point 4, 1 volt per division
Channel B:	Test Point 5, 1 volt per division
Both Channels:	A. C. coupled, Channels A and B added, Channel B inverted
Time Base:	50 milliseconds per division, synchronize internally on Channel A or B
Trigger:	Automatic

E. The minimum amplitude displayed on the scope should be no less than three (3) volts peak-to-peak at any point.

F. Reverify the measurement with another work diskette.

G. Check the upper and lower head, if applicable.

H. If the amplitude is less than the specification, inspect the heads to ensure they are not contaminated.

I. Clean the heads with a cleaning diskette if they are contaminated.

J. Replace the circuit board if cleaning does not improve the amplitude.

K. If replacing the circuit board does not correct the amplitude, replace the Head Carriage Assembly.

2.7 AZIMUTH CHECK

Azimuth is the angle of the heads with respect to the track at the point of the read/write gap. Azimuth is measured in minutes (one minute = 1/60 degree).

A. Set up an oscilloscope as follows:

Channel A:	Test Point 2, 100 mV per division
Channel B:	Test Point 3, 100 mV per division
Ground:	Test Point 1
Both Channels:	A. C. coupled, Channels A and B added, Channel B inverted
Time Base:	1 millisecond or as required to display the pulse groups
Trigger:	Leading edge of appropriate test point (see Section 2, Item Number 1)

B. Insert an alignment diskette.

C. Step the drive to Track 76.

D. Observe the following pattern. Figure 2-9 depicts an optimum head alignment of zero minutes of azimuth error. This means that the Head Carriage Assembly is perpendicular to the track being read, Track 76. Bursts 1 and 4 are of equal amplitude; Bursts 2 and 3 are of equal amplitude.

Note

Measure the azimuth burst. Ensure that Burst 1 is less than or equal to Burst 2, and that Burst 4 is less than or equal to Burst 3.

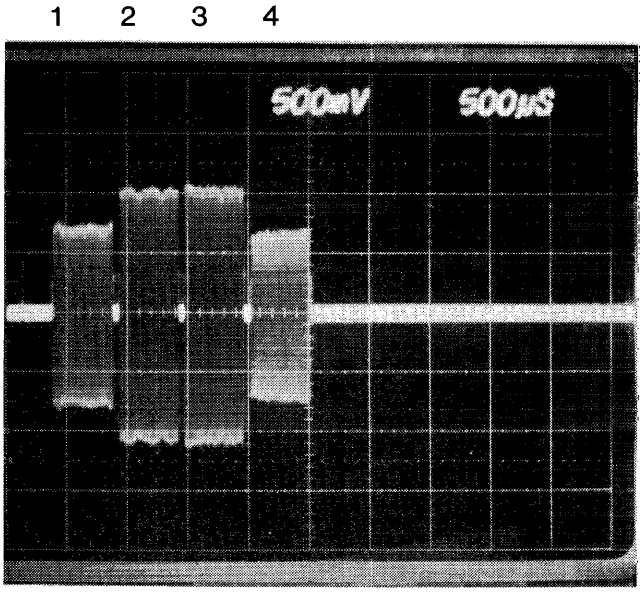


Figure 2-9

Optimum Head Azimuth Alignment

E. Figure 2-10 depicts an azimuth of exactly minus 9, 12, or 18 minutes, depending upon the manufacturer of the diskette used. This is the lower limit of allowable azimuth error. Bursts 1 and 2 are of equal amplitude. If this signal is observed, the Cats Eye alignment should be checked prior to any corrective action.

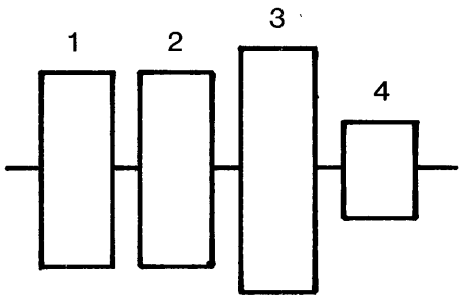


Figure 2-10
Head Azimuth of Acceptable Lower Limits

F. Figure 2-11 depicts an alignment of exactly plus 9, 12, or 18 minutes, depending upon the manufacturer of the diskette used. Bursts 3 and 4 are of equal amplitude. This is the upper limit of allowable azimuth error. If this signal is observed, the Cats Eye alignment should be checked prior to any corrective action.

G. After the lower head has been checked, switch to read on the upper head and observe the azimuth pattern. Both the upper and lower heads should be within the specification.

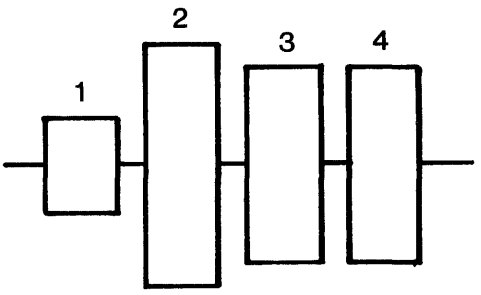


Figure 2-11
Head Azimuth Alignment of Acceptable Upper Limits

Note

The head's azimuth is not adjustable. It is suggested that the drive be sent to an authorized repair center or a new Head assembly be installed. In the latter case, all previous adjustments should be made again.

2.8 LOAD ARM ADJUSTMENT

This adjustment is made to ensure proper loading of the head when the diskette is engaged (see Figure 2-12).

A. Insert a work diskette into the drive.

B. Turn the diskette lever to load the disk, and seek to Track 00. There should be a space of .015 inch minimum between the head load arm and the load plate.

C. Seek to Track 76, and ensure that a space of .015 inch minimum remains between the head load arm and the load arm.

D. Adjust the screw located behind the head load cam until the foam just touches the platen.

E. Insert a work diskette and ensure that there is adequate space between the upper head and the diskette.

F. The upper head should not hit the diskette when inserting and ejecting it.

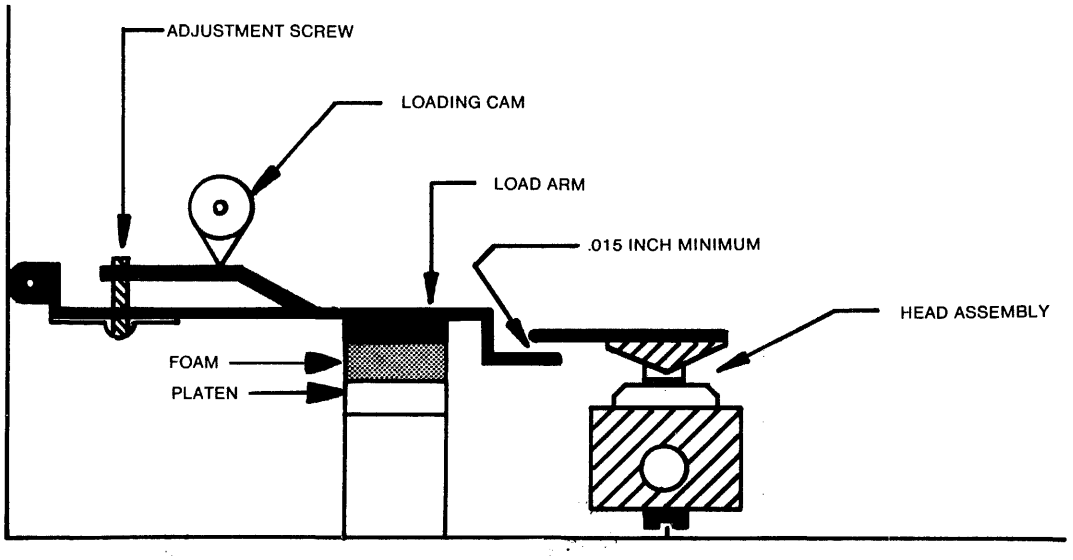


Figure 2-12
Load Arm Adjustment, Front View

SECTION III

PRINTED CIRCUIT BOARD OPERATION

3. INTRODUCTION

This section contains the interface description and the circuit board theory of operations for the TM848 family of disk drives. In addition, Sections 3.1 and 3.2 contain schematic diagrams of the circuit boards installed in the drive.

3.1 PHYSICAL DESCRIPTION OF THE CIRCUIT BOARD

The printed circuit board is approzimately 12.50-inches long by 5.25-inches wide. Figure 3-1 contains an illustration of the placement of test points and connectors.

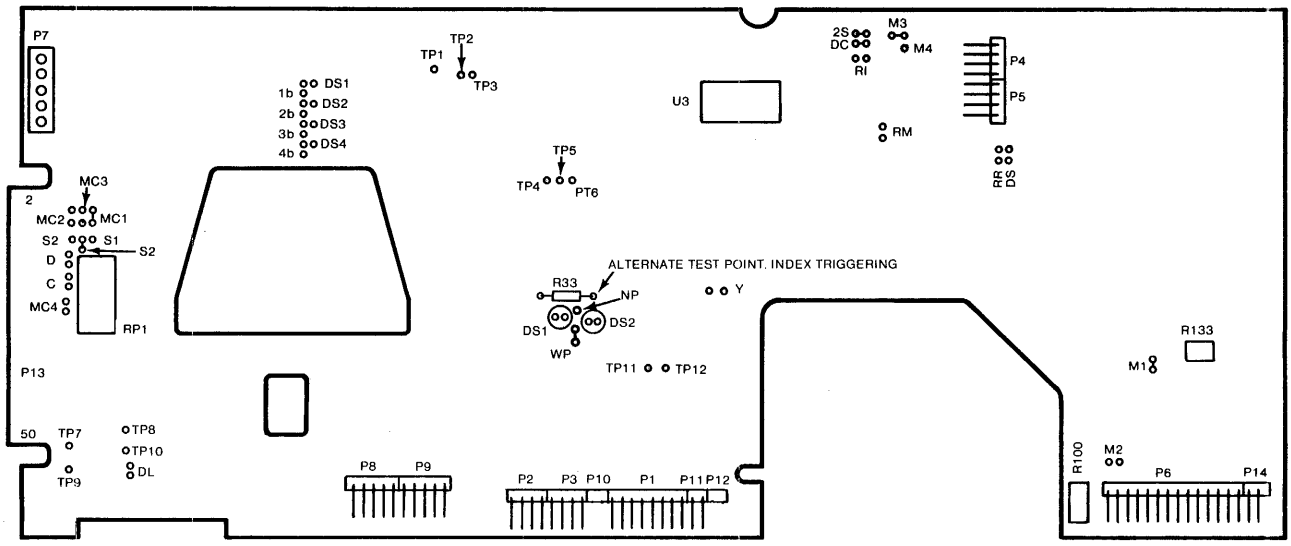


Figure 3-1
Printed Circuit Board

3.2 INTERFACE ELECTRONICS SPECIFICATIONS

All interface signals are TTL compatible. Logic true (low) is +0.4 volt minimum. Figure 3-2 illustrates the interface configuration. The maximum interface cable length is ten feet.

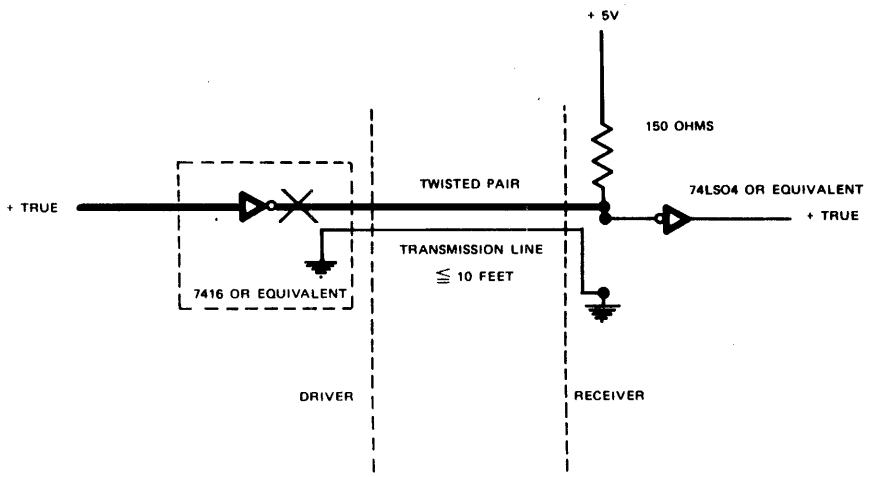


Figure 3-2
Interface Configuration

It is recommended that the interface cable be flat ribbon cable, with a characteristic impedance of 100 ohms.

Interface connector pin assignments are given in Table 3-1.

3.3 INPUT CONTROL LINES

A. DS1-DS4, Select Lines

Functional Description

The select lines (see Figure 3-3) provide a means of selecting and deselecting a drive. These four lines, DS1 through DS4, select one of the four drives attached to the controller. When the signal logic level is true (low), the drive electronics are activated, and the drive is conditioned to respond to Step or Read/Write commands. When the logic level is false (high), the input control lines and output status lines are disabled.

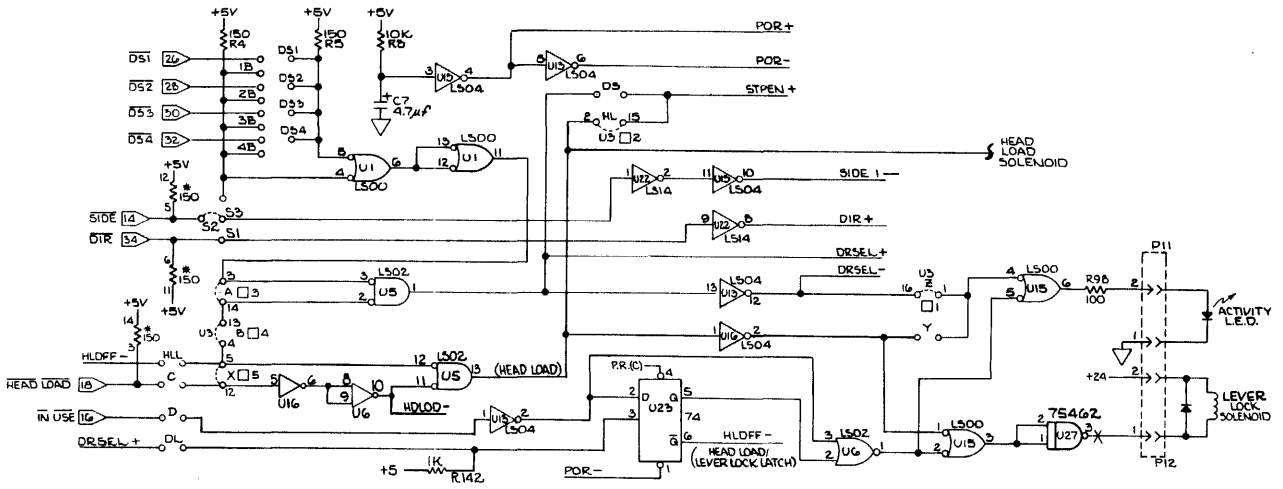


Figure 3-3
Select Lines Schematic Diagram

A select line must remain stable in the true (low) state until after a Step or Read/Write command has been executed.

The drive select address (1-4) is determined by shorting plugs on the circuit board. Select lines 1 through 4 provide a means of daisy chaining a maximum of four drives to a controller. Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more select lines are in the true (low) state simultaneously.

Circuit Description

An 150-ohm resistor holds the output of the appropriate Select line high (false) until the line is driven low (true). Then, the Select signal is gated through U1 and U5 to derive the signal DRSEL+. DRSEL+ is used to gate all I/O Port, ensuring that only one drive's data is present on the interface at a time. Writing and stepping are also gated by the signal DRSEL+. This signal is inverted by U13, then buffered by U15 to drive the Activity L. E. D., which is located on the front panel. Option Z is factory installed. It should be installed for the Activity L. E. D. to operate with Drive Select.

B. MOTOR ON, Drive Motor Enable

TABLE 3-1

DRIVE INTERFACE LINES AND PIN CONNECTORS

Ground	Pin Number	Signal
1	2	Write Current Switch
3	4	Motor Off Control 1
5	6	Motor Off Control 2
7	8	Motor Off Control 3
9	10	Two Sided (Strappable) (Model TM848-2 only)
11	12	Disk Change (Strappable)
13	14	Side Select (Model TM848-2 only)
15	16	Activity Indicator (Strappable)
17	18	Head Load Line
19	20	Index
21	22	Ready
23	24	Motor Off Control 4
25	26	Drive Select 1 (Side Select Option, TM848-2 only)
27	28	Drive Select 2 (Side Select Option, TM848-2 only)
29	30	Drive Select 3 (Side Select Option, TM848-2 only)
31	32	Drive Select 4 (Side Select Option, TM848-2 only)
33	34	Direction Select (Side Select Option, TM848-2 only)
35	36	Step
37	38	Write Data
39	40	Write Gate
41	42	Track 00
43	44	Write Protect
45	46	Read Data
47	48	Alternate I/O
49	50	Alternate I/O

Functional Description

The TM848 has a D. C. brushless motor that can be enabled in three ways:

1. By using the four radial Motor Control lines, MC1 through MC4.

2. By the Head Load line using shorting plug M4. Using this line enables all drives' Motor On lines.

3. By Drive Select, using shorting plug M3.

The Motor Control lines, MC1 through MC4, are true (low) signals that turn the motor off. Shorting plug M2 must be installed for these control lines to operate.

When a Motor Control line is false (high), the drive motor accelerates to its operational speed in less then 500 milliseconds. This keeps the spindle rotating at a constant speed of 360 RPM. When the Motor Control line is true (low) the motor coasts to a stop.

When using Head Load to enable the drive motor, M4 must be installed. All of the motors are enabled when the Head Load line goes true (low). M1 should be installed if a motor turn off delay is desired. See Section 1.19.21 for an additional description of this circuit.

When a Drive Select line is to be used for Motor Enable, M3 must be installed. This enables the drive motor when the Select line goes low.

Circuit Description

When the motor is enabled by any of the above, U35, Pin 6, floats high, allowing the speed control U41 to start the drive motor. Two Hall Effect transducers in the motor, supply the necessary feedback signals for proper speed regulation. When U35-6 goes high, the output of U41, Pin 6, turns on Q21, which in turn applies a varying voltage to Q20 that regulates the amount of current through Q20, and the motor driver transistors Q1 through Q4. Transistors Q1 through Q4 are turned on by the gated pulses derived from the conditioned outputs of the Hall Effect transducers. The conditioned output of U38, Pin2, is subsequently conditioned by Gate U36, which acts as an edge trigger and pulse doubler. This signal is fed back to U41, Pins 2 and 3, which results in closed loop speed control. The drive motor's rotational speed is approximately 2520 RPM, when adjusted, to give a spindle speed of 360 RPM.

C. DIR STEP, Direction and Step Lines

Functional Description

When the drive is selected, a true (low) pulse with a time duration between 200 nanoseconds and 2 milliseconds on the Step line initiates the track access motion. The direction of motion is determined by the logic state of the Direction line when a Step pulse is issued. The motion is toward the center of the drive if the Direction line is in the true (low) state when a Step pulse is issued. The direction of motion is away from the center of the drive if the Direction line is in the false (high) state when a Step pulse is issued. To ensure proper positioning, the Direction line should be stable for a minimum of 100 microseconds before the trailing edge of the corresponding Step pulse. The Direction line should also remain stable until 100 microseconds after the trailing edge of the Step pulse. The access motion is initiated on the trailing edge of the Step pulse.

When the carriage is positioned at Track 00 and the stepper motor is at Phase 0, the signal at Pin 42 of P13 goes true (low), indicating that Track 00 has been reached.

When stepping in or out, Test Point 8 is a high going pulse for each step pulse issued.

Circuit Description

The Direction line comes in on Pin 34 of the interface connector. A high signal directs the step logic to step toward Track 00. A low signal directs the step logic to step toward a higher numbered track.

The direction line sets the proper phase to the exclusive OR gates of U9.

TABLE 3-2

STEPPER LOGIC TRUTH TABLE

Step Out Toward Track 00

	Phase				
Pin No.	0	3	2	1	0
U21-9	0	1	1	0	0
U21-8	1	0	0	1	1
U21-5	0	0	1	1	0
U21-6	1	1	0	0	1

Step In Toward The Upper Tracks

	Phase				
Pin No.	0	1	2	3	0
U21-9	0	0	1	1	0
U21-8	1	1	0	0	1
U21-5	0	1	1	0	0
U21-6	1	0	0	1	1

The step pulses come in at Pin 36 of the interface connector. They are buffered by U22 and gated at U14 by the unit select, and the Not Write signal. The step pulses then go to the C inputs of the two flip flops at U21. The direction of the step, hence the selection of the flip flop to be toggled, is done by the two exclusive OR gates of U9. These gates are controlled by the step direction line and by the state of the two flip flop outputs.

The POR- ($\overline{\text{Power On Reset}}$) signal resets the two flip flops to Phase 0 after a Power On.

The output of the two flip flops drives the stepper motor through the drivers of U39, U40, and U12. The diodes, CR2-9, are for voltage spike elimination. The current through the stepper motor coils is reversed sequentially, one at a time.

D. $\overline{\text{WRT GATE}}$

Functional Description

When the Write Gate signal is true (low), the write electronics are prepared for writing data (read electronics disabled). This signal turns on the write current in the read/write head. Data is written under control of the Write Data input line. It is necessary for the Write Gate interface line to go low before the first Write Data pulse. However,the separation between the leading edge of Write Gate and the first significant Write Data pulse should not be less than two microseconds and not greater than four microseconds. The same restrictions exist for the relationship between the last Write Data pulse and the termination of the Write Gate signal. When the Write Gate line goes false (high), the trim erase will stay on for 550 microseconds (see Trim Erase, page 3-7).

When a write-protected diskette is installed in the drive, the write electronics are disabled, irrespective of the state of the Write Gate line. Check the list of options (see Section 1.19) for exceptions and further discussion of write protect options. Stepping is also disabled by a true (low) Write Gate.

Tandon Corporation recommends that the controller wait one millisecond after the $\overline{\text{WRT GATE}}$ goes high (false) before any step pulses are sent to the drive.

Circuit Description

A low (true) $\overline{\text{WRT GATE}}$ signal is applied to Pin 40 of the interface connector P13. This signal is

inverted and gated with Write Protect and Drive Select to enable U23, U30, and Q13. Transistors Q13 and Q12 are write current switches. Q13 and Q12 are on in parallel when the low Write Current interface is high (false). This results in a write current of 10 milliamps. When the low Write Current line goes low (true), transistor Q12 turns off, and the current decreases to 7 milliamps. R52 and R51 determine the amount of write current supplied to the head. The network CR18, CR19, CR20, R80 and R81 is a power-loss write disable. If a sudden voltage loss occurs, transistor Q14 turns off, disabling the write current.

E. $\overline{\text{WRT DATA}}$

Functional Description

When the drive is selected, the write data line provides the bit-serial Write Data pulses that control the switching of the write current in the heads. The write electronics must be conditioned for writing by the Write Gate line.

For each high-to-low transition on the $\overline{\text{WRT DATA}}$ line, a flux change is produced at the head write gap. This causes a flux change to be stored on the diskette (see Figure 3-4).

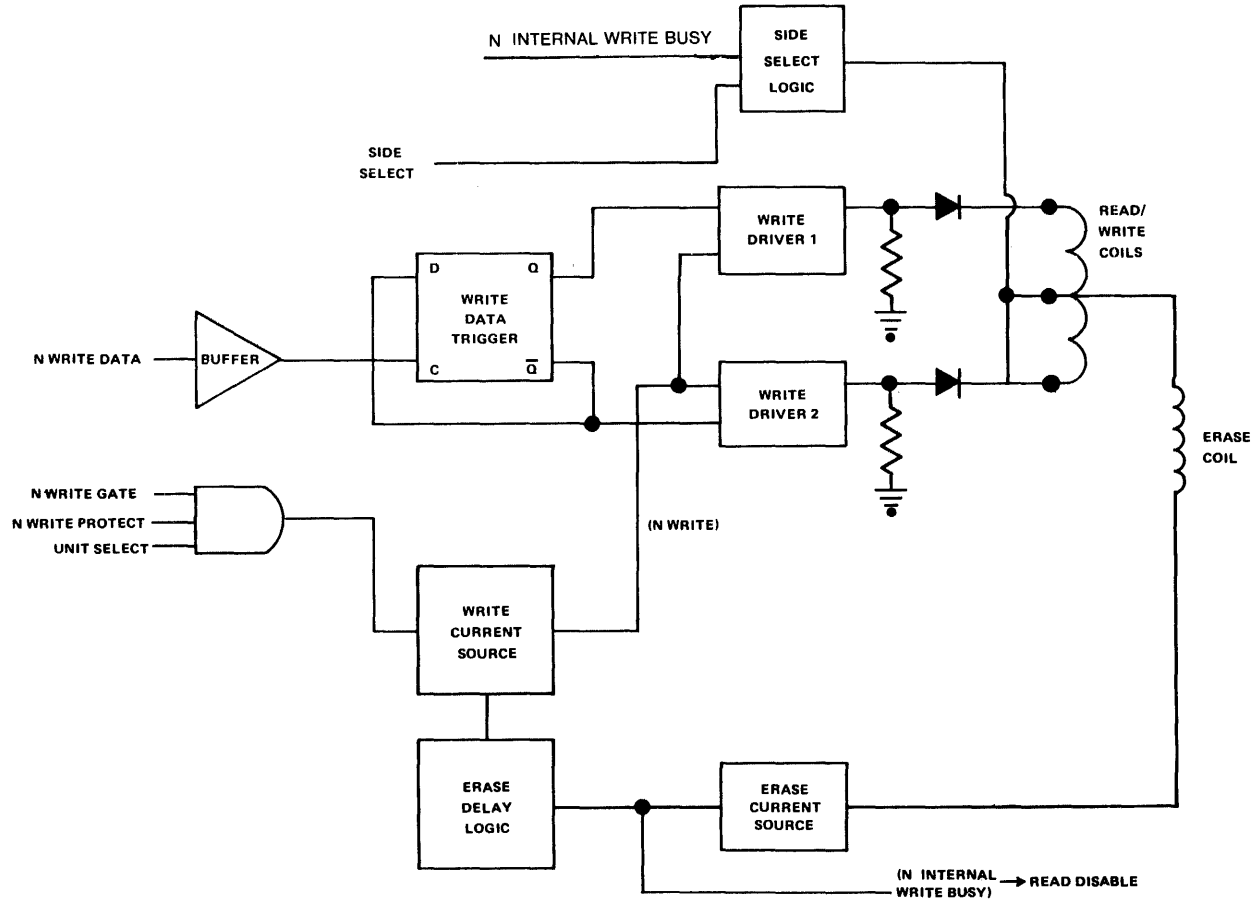


Figure 3-4
Write Data Circuit Block Diagram

When a double-frequency type encoding technique is used (in which data and clock form the combined Write Data signal), it is recommended that the repetition of the high-to-low transitions, when writing all zeros, be equal to the nominal data rate ±0.1 percent. The repetition rate of the high-to-low transitions, when writing all ones, should be equal to twice the nominal data rate ±0.1 percent. The data transfer rate for a 1F pattern is 250,000 Bits Per Second (BPS). The data transfer rate for a 2F pattern is 500,000 BPS.

Circuit Description

Data is sent to the drive via interface Pin 38. This signal is inverted by U22, and is used to clock the D flip flop U23. The outputs of U23 are inverted subsequently, and used to drive Q15 and Q17, which direct the write current to the correct winding.

F. TRIM ERASE

Functional Description

The TM848 uses a tunnel erase scheme to achieve trim erase, which is used to erase a guard band around the data tracks, allowing minor track offsets and minor misalignment without data errors occurring. The erase poles are staggered .036 inch behind the read/write poles. At a media rotational speed of 360 RPM, the tunnel erase method requires that the trim erase be delayed for 190 microseconds afer the start of writing and that it be continued for 550 microseconds after the end of writing the data. The two one shots in U30 provide these delay time intervals.

When the write gate goes low, U30, Pin 9, (A input), is triggered and a high to low to high transition of 190 us is generated. The write gate is also applied to U30 Pin 1 (A input). When the write data is applied to the $\overline{\text{WRT DATA}}$ line, U23 conditions the data which in turn generates the signal WRT TRAN+ (write transition+). This signal is then applied to U30 Pin 2, (B input) which is a positive triggered input. This clock will retrigger this one shot continuously until the last transition of the WRT TRAN+ and WRT GATE− occurs. At this time, the one shot stays on for an additional 550 us. These outputs (U30, Pins 12 and 13) are gated by U31 which is the trime erase gate. This output goes low whenever both inputs are high, causing the trim erase to be enabled (see Figure 3-5).

G. $\overline{\text{SIDE SELECT}}$

Functional Description

$\overline{\text{SIDE SELECT}}$ can be generated three ways. See the option listing, Section 1.19, for this information. As shipped from the factory, the side is selected using the $\overline{\text{SIDE SELECT}}$ interface line.

When the Side Select signal is low, Side 1 (the upper head) of the drive is selected for read/write operations. When this signal is high, Side 0 of the drive is selected (see Figure 3-6). The Side Select signal must be stable during an entire read or write operation. This signal is best implemented in synchronization with the Drive Select line signal.

Circuit Description

As shipped from the factory, the Side Select signal is received on Pin 14 of edge connector P13. This signal is received by U22, inverted, then inverted again by U13. The output of U13, Pin 10, generates the signal called Side 1−.

The Side 1− signal is applied to U13, Pin 9, and U24, Pin 13. The output of U13, Pin 8, is applied to U24, Pin 1. This output at Pin 2 of U24 is the opposite of U24, Pin 12. The resistor divider network sets up the biasing voltages to turn on and turn off the head select transistor, Q18 or Q19. The head biasing voltages seen across the collector resistors will be 5.2V D. C. when selecting a head for a read operation, 12V D.C. during a write operation, and 0V D. C. when the head is not selected. The emitter voltages on Q18 and Q19 will always be the opposite of each other, causing CT0 or CT1 (center tap 0, center tap 1) to be selected.

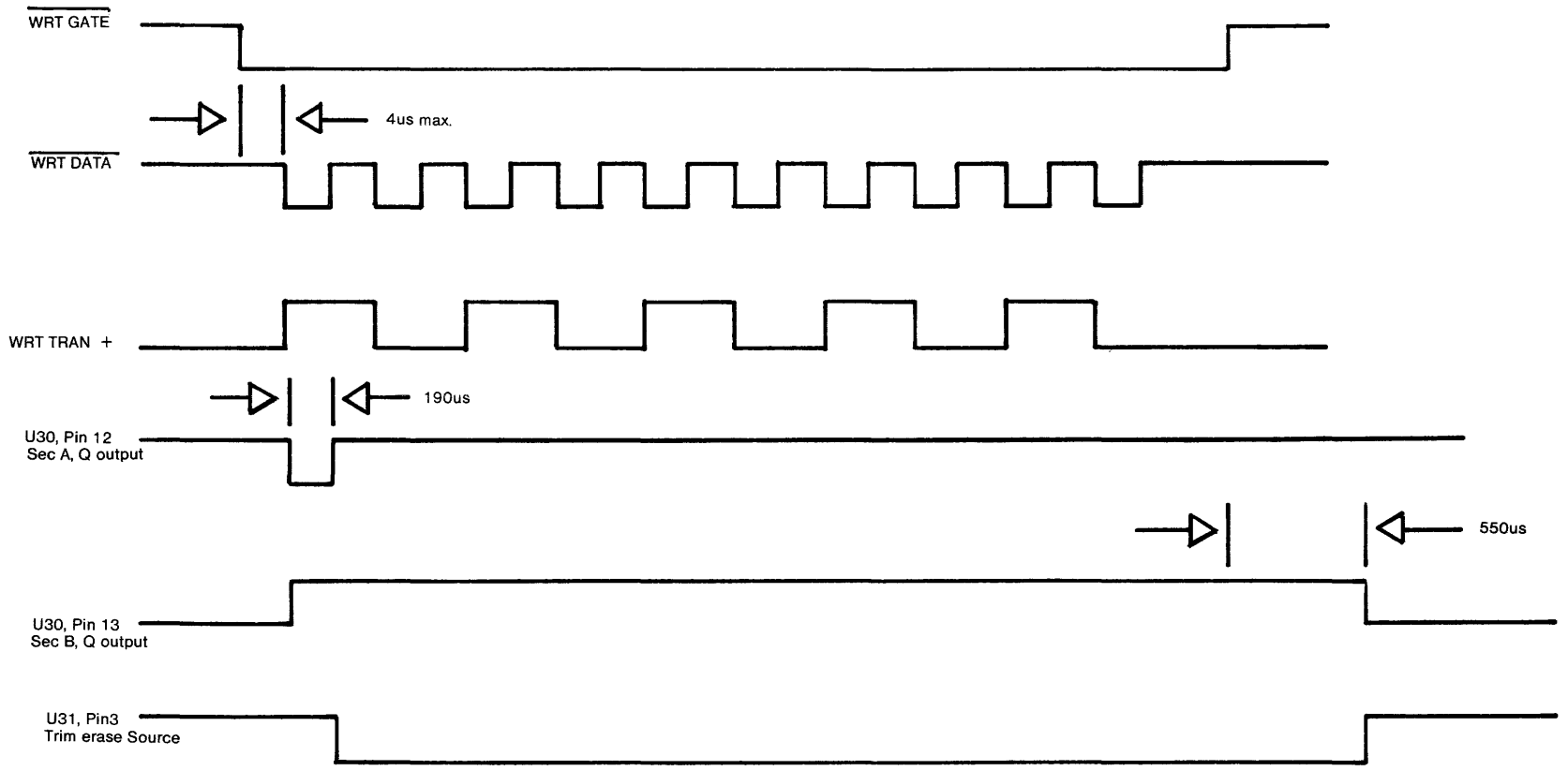


Figure 3-5
Trim Erase Diagram

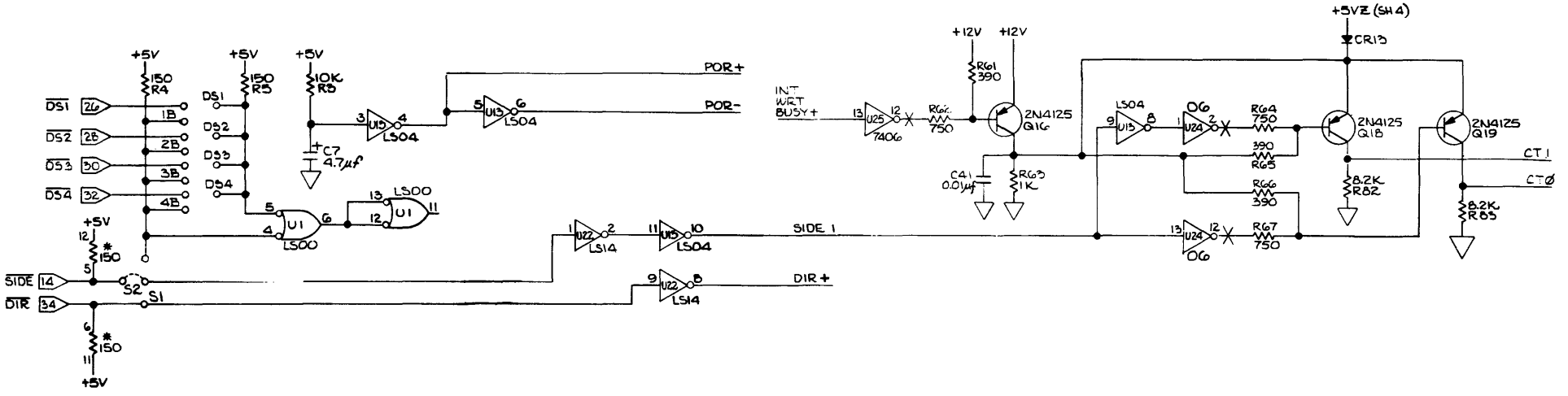


Figure 3-6
Side Select Schematic Diagram

3.4 OUTPUT CONTROL LINES

A. INDEX/SECTOR

Functional Description

The Index signal is provided once eash revolution (166.667 milliseconds nominal) to indicate the beginning of a track to the controller. The Index line remains in a low (true) state for the duration of the index pulse. The duration of the Index pulse is nominally 2.0 milliseconds. Two index sensors are supplied for use with single- or double-sided media.

The leading edge of an Index pulse is always used for timing to ensure diskette interchangeability between drives.

With a standard, soft-sectored diskette installed, the signal at R33 (see Figures 3-7 and 3-8) is a high going pulse, nominally 2.0 milliseconds in duration, every 166.667 milliseconds.

Circuit Description

Light from the Index L. E. D. is used to drive the index sensor, which is applied to the inverting input of U32. This signal is conditioned by U32, then inverted by U33. It is used to drive U26. Then the Respective index pulses are gated by U20, then with drive select by U4 to generate the signal index. U26 and the associated support integrated circuits U16 and U20 are configured to allow only the Index 1 signal to be present on the interface when a two-hole diskette envelope is used.

When a double-sided diskette is installed, the signal IN1FF+ is generated and gated by U4 to enable the output TWO SIDED.

B. Ready

Functional Description

Ready is used by the controller to ascertain the status of the drive. This signal is generated when the drive motor is on, the diskette installed, and the drive is selected. The signal takes less than 700 milliseconds to go true (low) from a motor start by Drive Select or Head Load (see Section 1.19.21).

Circuit Description

The index pulse is gated by U5, which in turn, triggers U17, a 220 millisecond retriggerable one shot. When the index-to-index time becomes less than 220 milliseconds, the one shot becomes continuously enabled and generates the signal SPIN—.

This signal is gated with POR+, Power On Reset, to enable the two-revolution counters U18. The output of U18, Pin 8, enables U6, whose output is gated with Drive Select to generate the signal ready. Whenever the drive motor is disabled, MTRON+ goes low, causing this sequence to be repeated when the motor is restarted.

C. Disk Change

Functional Description

The signal $\overline{\text{DISK CHANGE}}$ is used to indicate the host controller that a disk change operation has been made.

Circuit Description

The disk change flip-flop, U10, is reset by OPEN- whenever the lever is in the open position. When this occurs, U10-6 is high, and a true disk change status is sent to the interface on Pin 12 from U4-11. Flip-flop U10 is set on the trailing edge of drive select causing U10-6 to go low and setting the disk change status to the false state.

In actual use, this signal can be used by the host controller to determine that the diskette lever has been opened since the end of the previous drive select operation.

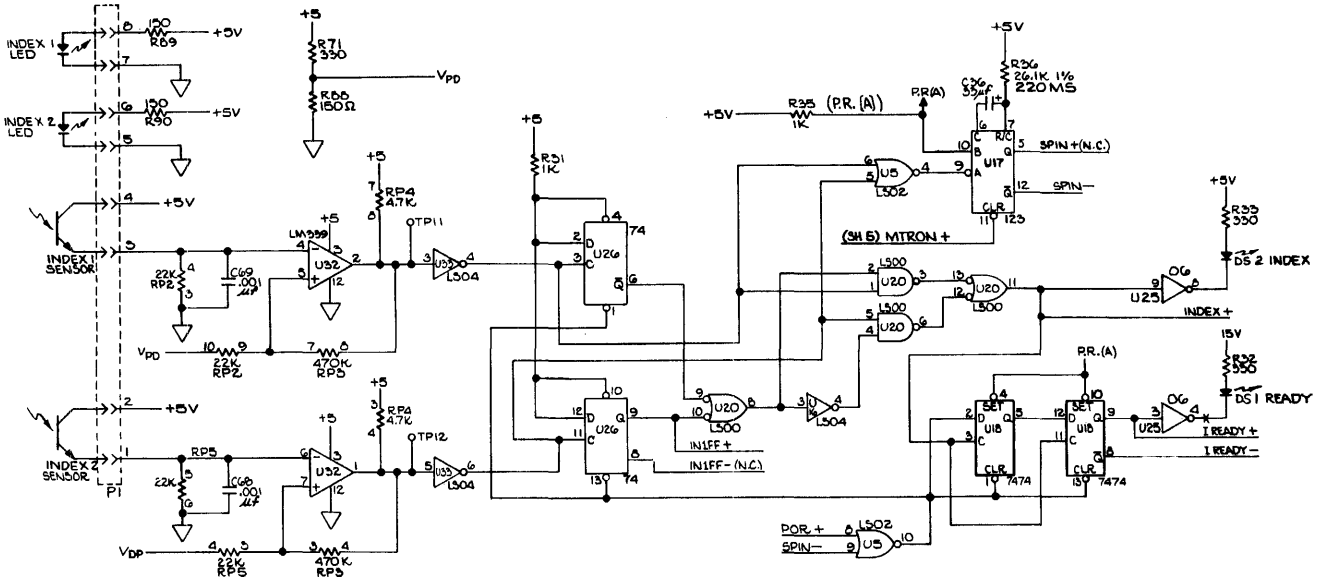


Figure 3-7
Index Schematic Diagram

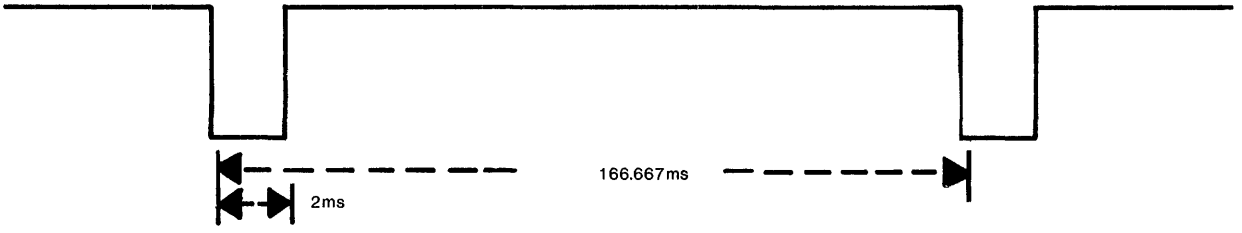


Figure 3-8
Waveform at Test Point 11 or 12
Alternate Test Point, R33
Soft Sectored Diskette Installed

D. TRK 00

Functional Description

When the drive is selected, the Track 00 interface signal indicates to the controller that the read/write head is positioned at Track 00. The Track 00 signal remains true (low) until the head is moved away from Track 00. The Track 00 sensor is activated internally between Tracks 2 and 3.

Interface Pin 42 (see Figure 3-9) is true (low) when the carriage is positioned at Track 00 and the step motor is at Phase 0.

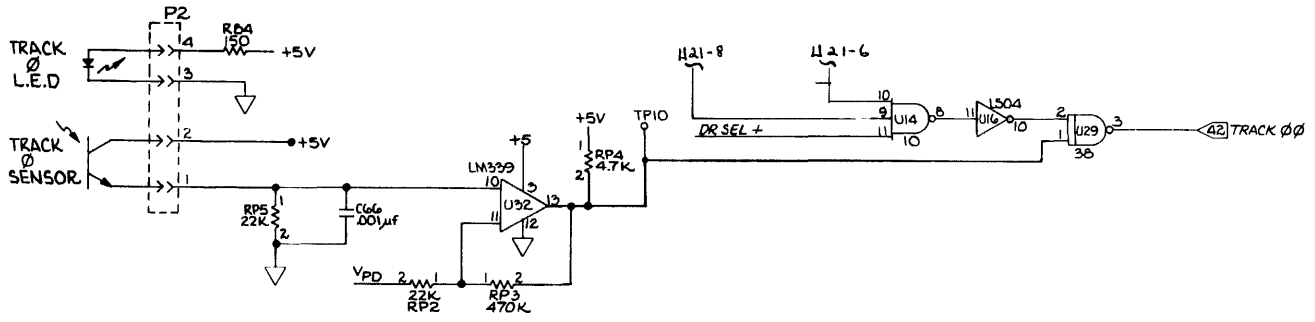


Figure 3-9
Track 00 Schematic Diagram

Circuit Description

When the read/write carriage is restored to Track 00, a tab on the carriage blocks light from the Track 00 L. E. D., turning off the Track 00 sensor transistor. This enables the inverting input of U32, a quad comparator causing U32, Pin 13, to go high.

This signal is gated with Phase 0 of the step circuit and with drive select to generate the signal $\overline{\text{TRK 00}}$. The signal at Test Point 10 should go high between Tracks 2 and 3, as the carriage is being moved toward $\overline{\text{TRK 00}}$.

E. WRITE PROTECT

Functional Description

When the drive is selected and the diskette is write protected, the $\overline{\text{WRITE PROTECT}}$ line's true (low). The write electronics are internally disabled when the diskette is write protected (see Option Listing for exceptions).

When the signal on the $\overline{\text{WRITE PROTECT}}$ line is false (high), the write electronics are enabled and the write operation can be performed. It is recommended that the controller not issue a Write command when the Write Protect signal is true (low).

It is recommended that the Write Data line be inactive whenever Write Gate is false (high).

Circuit Description

When a write protected diskette is installed, light from the Write Protect L. E. D. is detected by the Write Protected sensor transistor. The output of the sensor is high and is conditioned by U32. The output at Pin 14 is low generating the signal WR PROT-. This signal is used internally with the read/write circuitry. The signal WR PROT- is inverted by U33, and gated with DR SEL+ to generate the Write Protect signal.

F. READ DATA

Functional Description

The Read Data interface line transmits the read data to the controller when the drive is selected. It provides a pulse for each flux transition recorded on the media. The Read Data output line goes true (low) for a duration of 200 nanoseconds for each flux change recorded.

The leading edge of the low going, read data output pulse represents the true positions of the flux transitions on the diskette surface.

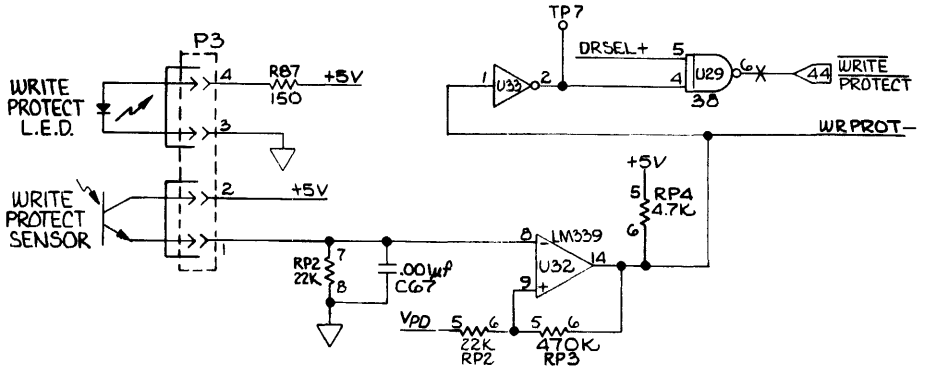


Figure 3-10
Write Protect Schematic Diagram

Test Points 2 and 3 (see Figure 3-11) are provided to observe the differential output of the first stage of Read signal preamplification. Test Points 4 and 5 are provided to observe the differential output of the second stage amplifier and differentiated Read signal. Test Point 9 is the output of the single shot used in the Read section, nominally 200 nanoseconds for each flux transition detected. Test Point 1 is signal ground.

Circuit Description

The read signal comes from the selected head on the drive. It is gated to the preamplifier U7 by the –Write signal to U25, which forward biases diodes CR14 and CR15. Then, the Read signal passes through a linear bandpass filter. The Read signal is then input to U2, the differentiator.

The output of U2 goes through the D. C. blocking capacitors to the crossover detector, U8, which digitizes the signal. This converts the signal into standard TTL level Integrated circuits U9, U11, and U10 comprise a comparator circuit. Any pulses that occur outside of the normal duty cycle of U11 are eliminated. U9 is an edge detector. U11 acts as a one shot, with a timeout of approximately 860 nanoseconds. U10 is the actual comparator.

The Read signal is presented to U9. Then it goes to U11, where the pulses are shaped to 200 nanoseconds. This output is gated at U29 with the Unit Select signal to produce a digital output at Pin 46 of the interface connector (see Figure 3-12).

Note

U11, the final one shot, is disabled when the drive is writing data onto the diskette.

G. Two Sided

Functional Description

This output enables the controller to determine if a diskette is installed, which utilizes the Index 2 index hole. This may be used to indicate to the host controller that a two-sided diskette is in the drive.

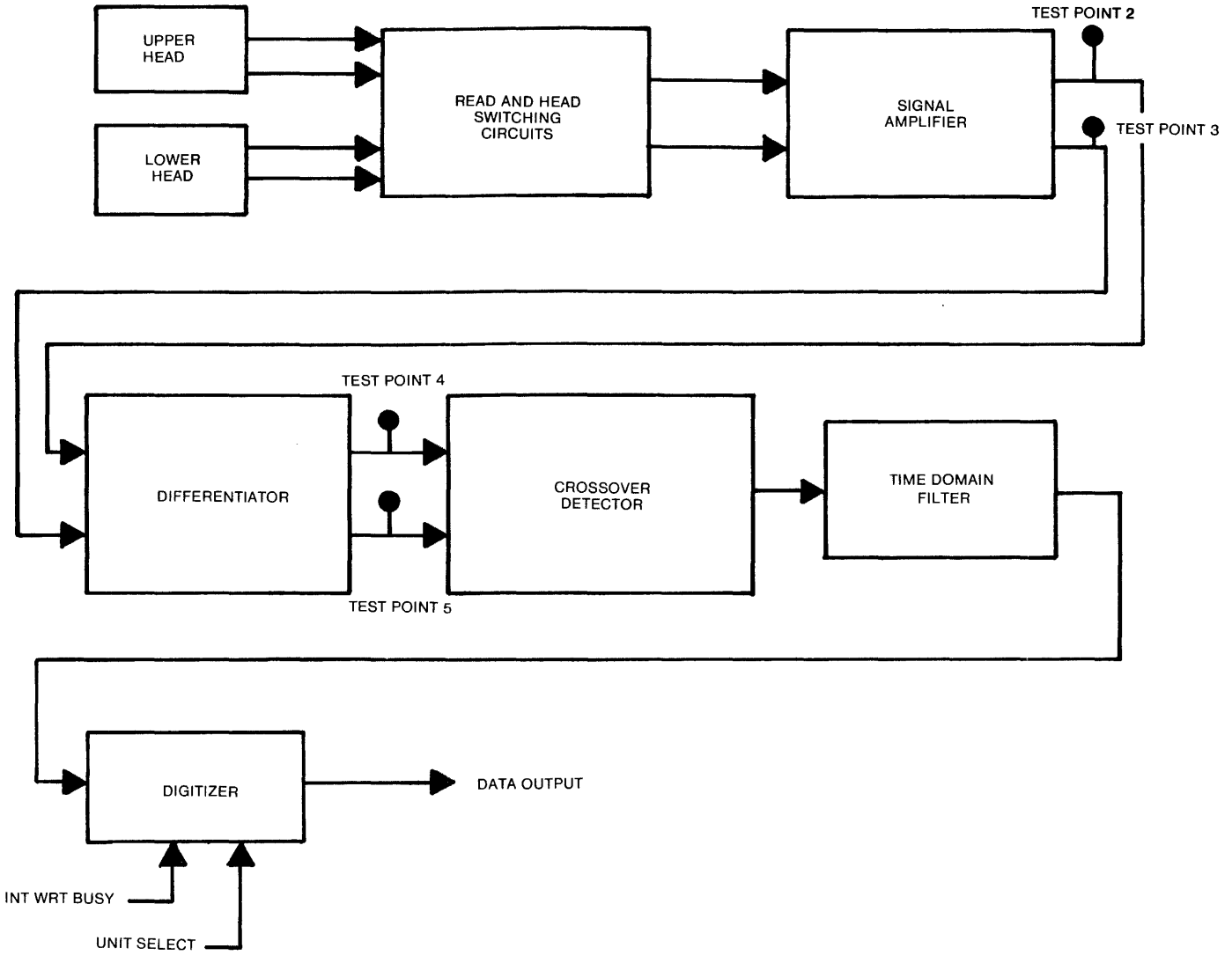


Figure 3-11
Read Circuit Block Diagram

Circuit Description

When a two-sided diskette is installed, the signal IN1FF+ is generated and gated by U4 to enable the low-going output Two Sided. The IN1FF signal also goes to the ready circuitry at U6-5 to disable Ready in the event that the upper head (Head 1) is selected when a single-sided (Head 0) diskette is installed (see Option RM for further discussion).

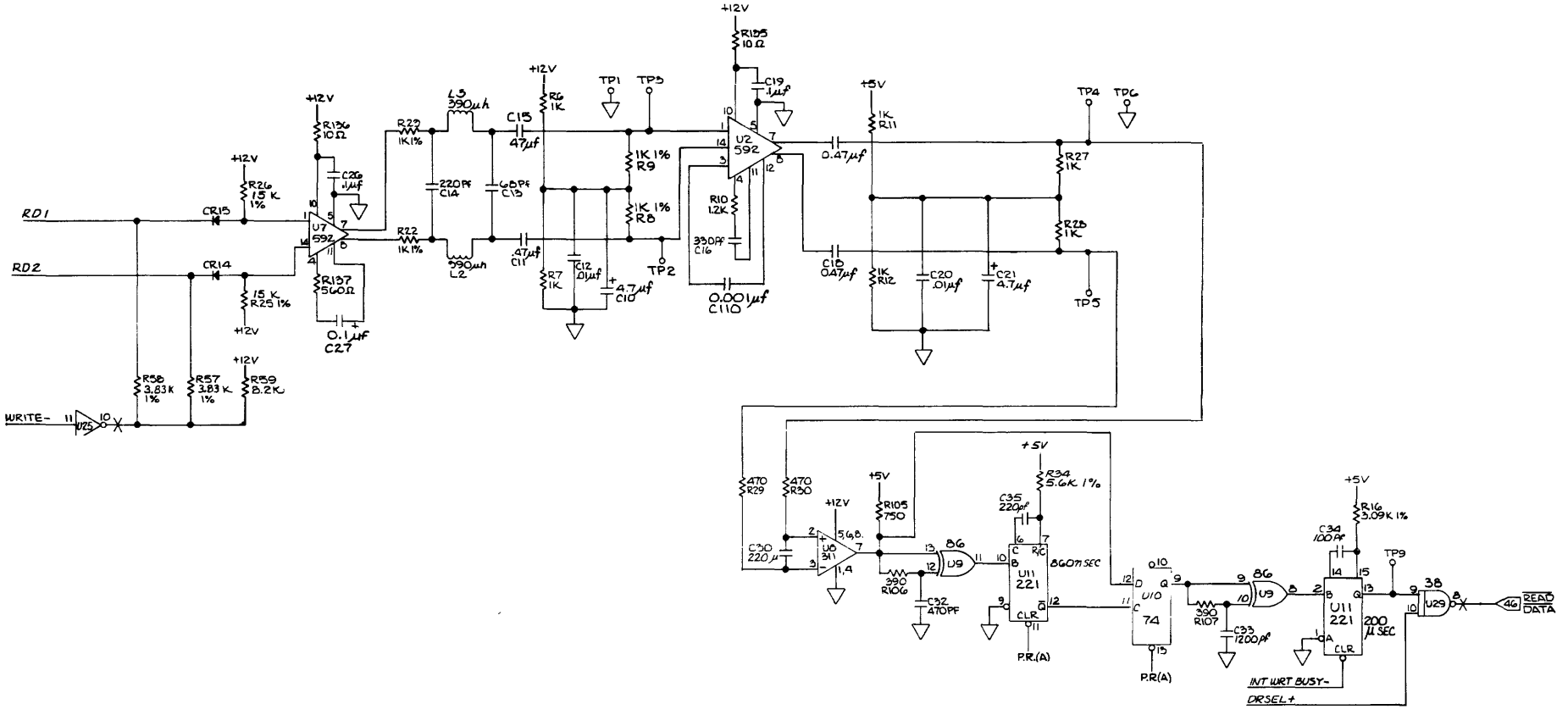


Figure 3-12
Read Data Schematic Diagram